

CLAIMS

What is claimed is:

- 1 1. A method comprising:
2 detecting an error of a transmission of an interconnect;
3 retrying the transmission in response to the detected error;
4 detecting a hard failure if the retrying is unsuccessful; and
5 reducing a transmission width of the interconnect in response to the detected
6 hard failure.

- 1 2. The method according to claim 1, wherein the reducing of the transmission width
2 comprises selecting a working portion of the interconnect in response to the hard failure.

- 1 3. The method according to claim 1, wherein the detecting of the hard failure
2 provides an indication of failed portions of the interconnect, and the reducing selects a
3 working portion of the interconnect based on the indication of failed portions.

- 1 4. The method according to claim 1, wherein the detecting of the transmission error
2 is performed using a cyclic redundancy check.

- 1 5. The method according to claim 1, further comprising replacing the interconnect
2 with a replacement interconnect after the transmission width is reduced.

1 6. The method according to claim 1, further comprising retrying the transmission
2 after the transmission width is reduced.

1 7. The method according to claim 1, wherein the interconnect is a bus.

1 8. An apparatus comprising:
2 a transmission error detector to detect an error of a transmission of an
3 interconnect;
4 a transmitting agent to retry the transmission in response to the detected error;
5 a hard failure detector to detect a hard failure of the interconnect if the retry is
6 unsuccessful; and
7 a transmission width reducer to reduce a transmission width of the interconnect
8 in response to the hard failure detector.

1 9. The apparatus according to claim 8, wherein the transmission width detector is to
2 select a working portion of the interconnect in response to the hard failure detector.

1 10. The apparatus according to claim 8, wherein the hard failure detector is to
2 indicate failed portions of the interconnect, and the transmission width detector is to
3 select a working portion of the interconnect based on the indicated failed portions.

1 11. The apparatus according to claim 8, wherein the transmission error detector is to
2 perform a cyclic redundancy check.

1 12. The apparatus according to claim 8, the transmitting agent to retry the
2 transmission after the transmission width is reduced.

1 13. The apparatus according to claim 8, wherein the interconnect is a bus.

1 14. The apparatus according to claim 8, wherein the interconnect is an input/output
2 bus.

1 15. An interconnect comprising:
2 a transmission width to transmit information;
3 a transmission error detector to detect a transmission error of the interconnect;
4 a transmitting agent to retry a transmission in response to the detected error;
5 a hard failure detector to detect a hard failure of the interconnect if the retry is
6 unsuccessful; and
7 a transmission width reducer to reduce a transmission width of the interconnect
8 in response to the hard failure detector.

1 16. The interconnect according to claim 15, wherein the transmission width detector
2 is to select a working portion of the interconnect in response to the hard failure detector.

1 17. The interconnect according to claim 15, wherein the hard failure detector is to
2 indicate failed portions of the interconnect, and the transmission width detector is to
3 select a working portion of the interconnect based on the indicated failed portions.

1 18. The interconnect according to claim 15, wherein the transmission error detector
2 is to perform a cyclic redundancy check.

1 19. The interconnect according to claim 15, the transmitting agent to retry the
2 transmission after the transmission width is reduced.

1 20. The interconnect according to claim 15, wherein the interconnect is a bus.

1 21. The interconnect according to claim 15, wherein the interconnect is an
2 input/output bus.

1 22. A system comprising:
2 a first component;
3 a second component; and
4 an interconnect comprising:
5 a transmission width to transmit information between the first component
6 and the second component;
7 a transmission error detector to detect a transmission error of the
8 interconnect;
9 a transmitting agent to retry a transmission in response to the detected
10 error;

11 a hard failure detector to detect a hard failure of the interconnect if the
12 retry is unsuccessful; and
13 a transmission width reducer to reduce a transmission width of the
14 interconnect in response to the hard failure detector.

1 23. The system according to claim 22, wherein the transmission width detector is to
2 select a working portion of the interconnect in response to the hard failure detector.

1 24. The system according to claim 22, wherein the hard failure detector is to indicate
2 failed portions of the interconnect, and the transmission width detector is to select a
3 working portion of the interconnect based on the indicated failed portions.

1 25. The system according to claim 22, wherein the transmission error detector is to
2 perform a cyclic redundancy check.

1 26. The system according to claim 22, the transmitting agent to retry the
2 transmission after the transmission width is reduced.

1 27. The system according to claim 22, wherein the interconnect is a bus.

1 28. The system according to claim 22, wherein the interconnect is an input/output
2 bus.

1 29. The system according to claim 22, wherein the first component is a processor, a
2 memory, a chip set, a memory bridge, an I/O device or an I/O hub and the second
3 component is a processor, a memory, a chip set, a memory bridge, an I/O device or an
4 I/O hub.